the first semiconductor die and the second semiconductor die. The semiconductor structure includes a molding compound between the first semiconductor die and the second semiconductor die. A first portion of a metal structure over a surface of the three dimensional stack and contacting a backside of the second semiconductor die and a second portion of the metal structure over the surface of the three dimensional stack and configured for electrically connecting the three dimensional stack with an external electronic device.

In some embodiments, the semiconductor structure includes a conductive plug between the metal structure and the first semiconductor die. In some embodiments, the semiconductor structure includes a dummy bump connected with the first portion of the metal structure, wherein the dummy bump is configured to connect with a dummy pattern external to the three dimensional stack.

In some embodiments, the semiconductor structure includes a plurality of bumps configured for electrically connected to a printed circuit board (PCB). In some embodiments, the semiconductor structure includes a PPI on the first semiconductor die and electrically coupled to the first semiconductor die.

A method of manufacturing a semiconductor structure includes several operations. One of the operations is providing a substrate. One of the operations is forming a circuitry on the substrate. One of the operations is flip bonding a semiconductor die with the circuitry with a bump. One of the operations is forming a conductive plug with a first end connected with the circuitry. One of the operations is exposing a passive surface of the semiconductor die and a second end of the conductive plug. One of the operations is forming a metal structure on the backside of the semiconductor die and the second end of the conductive plug.

In some embodiments, the method includes disposing a molding compound on the substrate to surround the semiconductor die and the conductive plug.

In some embodiments, the method includes performing a grinding operation to remove a portion of the molding compound to expose a passive surface of the semiconductor die and a second end of the conductive plug.

In some embodiments, the method includes disposing a dummy bump on a portion of the metal structure.

In some embodiments, the method includes forming a PPI in the circuitry.

In some embodiments, the method includes forming a patterned photo resist on the substrate for forming the conductive plug.

Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As those skilled in the art will readily appreciate form the disclosure of the present disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present disclosure.

Accordingly, the appended claims are intended to include within their scope such as processes, machines, manufacture, and compositions of matter, means, methods or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the invention.

What is claimed is:

1. A semiconductor structure, comprising:

a substrate and a first circuit on the substrate;

a metal structure comprising an active portion and a dummy portion, the active portion electrically coupled with the first circuit through a conductive plug, the dummy portion not being electrically coupled with any circuitry, the active portion and the dummy portion being on a same level of the metal structure;

a semiconductor die bonded to the substrate through a first active bump via a conductive pad on an active surface of the semiconductor die, a passive surface of the semiconductor die contacting the dummy portion of the metal structure, wherein the passive surface is opposite to the active surface;

a dummy bump connected to the dummy portion of the metal structure; and

a molding compound between the substrate and the active surface of the semiconductor die and surrounding the conductive plug;

wherein the dummy bump is surrounded by ambient air.

2. The semiconductor structure of claim **1**, wherein the dummy bump is configured to dissipate heat from the passive surface.

3. The semiconductor structure of claim **1**, wherein the active portion of the metal structure further comprises a redistribution layer (RDL) connecting to one end of the conductive plug.

4. The semiconductor structure of claim **1**, wherein the dummy portion of the metal structure further comprises an under bump metal (UBM) for receiving the dummy bump.

5. The semiconductor structure of claim **1**, further comprising a second active bump connected to the active portion of the metal structure.

6. The semiconductor structure of claim **1**, wherein the first circuit circuitry includes a post passivation inductor (PPI).

7. The semiconductor structure of claim **6**, wherein the PPI is connected to one end of the conductive plug.

8. The semiconductor structure of claim **1**, wherein the conductive pad is an under bump metal (UBM), and the conductive pad is connected to an interconnection of the semiconductor die.

9. The semiconductor structure of claim **1**, wherein the substrate includes a semiconductor device.

10. A semiconductor structure, comprising:

a three dimensional stack comprising:

a first semiconductor die;

a second semiconductor die electrically connected with the first semiconductor die with a first active bump positioned on a frontside of the second semiconductor die; and

a molding compound between the first semiconductor die and the second semiconductor die;

wherein a dummy portion of a metal structure being over a surface of the three dimensional stack and contacting a backside of the second semiconductor die, the dummy portion neither being electrically coupled to the first semiconductor die nor to the second semiconductor die;

a dummy bump connected with the dummy portion of the metal structure, the dummy bump being surrounded by ambient air; and

an active portion of the metal structure over the surface of the three dimensional stack, not contacting the backside of the second semiconductor die, and configured for electrically connecting the three dimensional stack with an external electronic device, wherein the active portion and the dummy portion are in a same level of the metal structure.